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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,984	11/25/2003	Mukta G. Farooq	END920030114US1	6936

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EXAMINER

WILLIAMS, ALEXANDER O

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/721,984	Applicant(s) FAROOG ET AL.	
	Examiner Alexander O. Williams	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 September 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 6-20 is/are rejected.
- 7) ☒ Claim(s) 4 and 5 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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Serial Number: 10/721984 Attorney's Docket #: END920030114US1

Filing Date: 11/25/2003;

Applicant: Farooq et al.

Examiner: Alexander Williams

Applicant's RCE filed 9/6/06 has been acknowledged.

Applicant's Amendment filed 8/7/06 to the election with traverse of species I, figure 2, claims 1-20, filed 10/27/05, has been acknowledged.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3, 6-8, 10, 11, 13, 14, 16-18 and 20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Brodsky (U.S. Patent # 7,083,436 B2).

1. Brodsky (figures 1 and 2) show a semiconductor module, comprising: a semiconductor chip (**inherent**); a substrate (**inherent**); and an interposer structure **10** having a connection only to the semiconductor chip and to the substrate, wherein the interposer structure includes an elastomeric compliant material having metallurgical **14** through connections having a predetermined shape, wherein the metallurgical through connections form the only connection to the semiconductor chip and to the substrate.
2. The semiconductor module of claim 1, Brodsky show wherein the elastomeric, compliant material has the metallurgical through connections being one of the group consisting of: embedded and positioned therein.
3. The semiconductor module of claim 1, Brodsky show wherein the predetermined shape is selected from the group consisting of spherical, elongate, c-shaped, s-shaped and ellipsoid.
6. The semiconductor module of claim 1, Brodsky further comprising underfill **14** for sealing the interposer structure between the semiconductor chip and the substrate.
7. The semiconductor module of claim 1, Brodsky show wherein the metallurgical through connections of the interposer structure electrically connect an under bump metallization of the semiconductor chip to a top surface metallization of the substrate.
8. The semiconductor module of claim 7, Brodsky show wherein the metallurgical through connections are soldered to at least one of the under bump metallization or the top surface metallization.
10. Brodsky (figures 1 and 2) show a semiconductor module, comprising: a semiconductor chip (**inherent**) having an under bump metallization; a substrate

(inherent) having a top surface metallization; and an interposer structure **10** only in contact with the under bump metallization and the top surface metallization, wherein the interposer structure comprises an elastomeric, compliant material that includes metallurgical through connections having a predetermined shape, wherein the metallurgical through connections form the only connections to the under bump metallization and to the top surface metallization.

11. The semiconductor module of claim 10, Brodsky show wherein the predetermined shape is selected from the group consisting of spherical, elongate, c-shaped, s-shaped and ellipsoid.

13. The semiconductor module of claim 10, Brodsky further comprising underfill **14** for sealing the interposer structure between the semiconductor chip and the substrate.

14. The semiconductor module of claim 10, Brodsky show wherein the metallurgical through connections are soldered to at least one of the under bump metallization or the top surface metallization.

16. Brodsky (figures 1 and 2) show a method for forming a semiconductor module, comprising: embedding metallurgical **14** through connections within an elastomeric, compliant material to form an interposer structure **10**; and positioning the interposer structure between a semiconductor chip **(inherent)** and a substrate **(inherent)** to electrically connect and only contact the semiconductor chip to the substrate, wherein the metallurgical through connections form the only contact to the semiconductor chip and to the substrate.

17. The method of claim 16, Brodsky show wherein the metallurgical **114** through connections electrically connect an under bump metallization **104** of the semiconductor chip to a top surface metallization of the substrate.

18. The method of claim 17, Brodsky further comprising soldering the interposer structure to at least one of the under bump metallization or the top surface metallization.

20. The method of claim 16, Brodsky further comprising sealing the interposer structure between the semiconductor chip and the substrate with underfill **14**.

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(9) In the typical injection method, an elastomeric mixture containing the conductive particles is injected through via 108 where it then passes through passages 106 in non-conductive carrier sheet 114 and stops in the lower half of the mold. As a result of the injection of the conductive elastomer into the mold cavity, any air contained within the mold is displaced. This displacement of the air within the mold cavity results in venting of the air along the intersection of the two mold sections as it is the primary avenue for escape. The venting along the non-conductive carrier sheet allows some of the elastomer mixture to escape along the non-conductive carrier sheet, which results in a condition commonly referred to in the art as "mold flash." The occurrence of mold flash prevents the use of smaller and more electrically efficient materials in constructing the interconnect elements, thus negatively affecting the potential electrical performance of the interposer.

(7) Referring now to the drawings wherein like reference numerals refer to like parts throughout, there is seen in FIG. 2 an interposer, designated generally by reference numeral 10, comprising a non-conductive carrier sheet 12 and conductive interconnect members 14. Non-conductive carrier sheet 12 is a conventional insulator material used in flexible circuits, e.g., a polyimide such as DuPont Kapton.RTM. or a polyester such as DuPont Mylar.RTM., with an array of passages 16, as illustrated in FIG. 3, that extend completely though the sheet in a predetermined pattern. **The passages 16 containing the conductive interconnect elements 14 can be arranged to correspond to the electrical contacts on a chip and a printed circuit board to which the chip, for instance, is to be attached.**

Claims 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brodsky (U.S. Patent # 7,083,436 B2) in view of Shih et al. (U.S. Patent # 6,286,208 B1).

Brodsky show the features of the claimed invention as detailed above, but fail to explicitly show support posts positioned adjacent the interposer structure, wherein the support posts support a heat spreader over the semiconductor chip.

Shin et al. is cited for showing interconnection with contact pads having enhanced durability. Specifically, Shih et al. (figures 1 to 21) specifically figure 9 show a semiconductor module **59**, comprising: a semiconductor chip **30**; a substrate **65**; and an interposer structure **10** electrically connecting the semiconductor chip to the substrate, wherein the interposer structure includes metallurgical **22** through connections having a predetermined shape and further comprises support posts **56** positioned adjacent the interposer structure, wherein the support posts **56** support a heat spreader **55** over the semiconductor chip for the purpose of providing an improved electrical connecting device.

12. The semiconductor module of claim 10, Shih et al. further comprises support posts **56** positioned adjacent the interposer structure for supporting a heat spreader **55** over the semiconductor chip.

19. The method of claim 16, Shih et al. further comprising positioning support posts **56** adjacent the interposer structure to support a heat spreader **55** over the semiconductor chip.

Therefore, it would be obvious to one of ordinary skill in the art to use Shih et al.'s structure to modify Brodsky's structure for the purpose of providing an improved electrical connecting device.

Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response

Applicant's arguments filed 9/6/06 have been fully considered, but are moot in view of the new grounds of rejections detailed above.


The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/712,713,713,717,720,704,710,675,773,774,778,734,7 37,738,780,e23.067,e23.101,e23.194,e21.503,e23.067 324/754,758,757,765, 174/255,256,260,261 361/748,760,761,762,767,769,771 439/65,66,91	12/11/05 5/19/06 9/18/06
Other Documentation: foreign patents and literature in 257/712,713,713,717,720,704,710,675,773,774,778,734,7 37,738,780,e23.067,e23.101,e23.194,e21.503,e23.067 324/754,758,757,765, 174/255,256,260,261 361/748,760,761,762,767,769,771 439/65,66,91	12/11/05 5/19/06 9/18/06
Electronic data base(s): U.S. Patents EAST	12/11/05 5/19/06 9/18/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
9/18/06